CLAIMS

1. (amended) A semiconductor nonvolatile storage circuit including first and second MISFETs,

source terminals of the first and second MISFETs connecting to a ground potential,

gate terminals of the first and second MISFETs connecting to a first word line,

a drain terminal of the first MISFET connecting to a bit line, and

a drain terminal of the second MISFET connecting to a differential pair line of the bit line,

the semiconductor nonvolatile storage circuit comprising:

a first switching element to electrically open/close a path between the drain terminal of the first MISFET and the bit line;

a second switching element to electrically open/close a path between the drain terminal of the second MISFET and the differential pair line and

wherein a conduction resistance value of the first or second MISFET is changed so that conduction resistance values of the first and second MISFETs differ from each other by applying an intermediate voltage between a power supply potential and a ground potential to the first word

line and by applying the power supply potential to any one of the bit line and the differential pair line of the bit line, whereby "1" or "0" is stored in accordance with the difference between the conduction resistance values.

2. The semiconductor nonvolatile storage circuit according to Claim 1,

wherein the first and second switching elements are third and fourth MISFETs, and

wherein gate terminals of the third and fourth MISFETs connect to a second word line.

3. The semiconductor nonvolatile storage circuit according to Claim 1 or 2,

wherein the drain terminals of the first and second MISFETs connect to the ground potential via third and fourth switching elements, respectively.

4. The semiconductor nonvolatile storage circuit according to Claim 3,

wherein the third and fourth switching elements are fifth and sixth MISFETs, and

wherein gate terminals of the fifth and sixth MISFETs connect to a differential pair line of the second word line.

5. The semiconductor nonvolatile storage circuit according to any of Claims 2 to 4, further comprising:

a volatile storage circuit whose one storage node connects to the bit line and the other storage node connects to the differential pair line of the bit line,

wherein a drain terminal of the third MISFET connects to the one storage node of the volatile storage circuit,

wherein a drain terminal of the fourth MISFET connects to the other storage node of the volatile storage circuit,

wherein the one storage node and the other storage node of the volatile storage circuit connect to each other via a fifth switching element, and

wherein a ground line of the volatile storage circuit connects to the ground potential via a sixth switching element.

6. (cancelled)

inverter circuit including an n-type driving transistor MN1 and a p-type load transistor MP1 and a second inverter circuit including an n-type driving transistor MN2 and a p-type load transistor MP2, and data of "1" or "0" is stored in the storage nodes C and C_.

[0014] The storage nodes C and C_ connect to a pair of bit lines BL and BL_ via transfer transistors MNT1 and MNT2, respectively. Gate terminals of the transfer transistors MNT1 and MNT2 connect to a word line WL. The paths between the storage nodes C and C_ and the pair of bit lines BL and BL_ are electrically opened/closed by a signal of the word line WL.

[0015] The known circuit SC includes the first MISFET MNM1 forming a source-drain path between the storage node C of the static semiconductor memory SM and a ground potential (GND) and the second MISFET ~~MNM1~~MNM2 forming a source-drain path between the storage node C_ and the ground potential (GND). Gate terminals of the first and second MISFETs MNM1 and MNM2 connect to a word line WLW.

[0016] A transistor MPEQ is a switching element to open/close the connection between the storage nodes C and C_ by using a signal line EQ. A transistor MNRS is a switching element to open/close the connection between the driving transistors MN1 and MN2 and the ground potential GND by using a signal line RESTORE.